ABSTRACT OF THE INVENTION

In testing of a plurality of logic circuits having the same function and included in an integrated circuit, an address decoder makes two logic circuits having the same function simultaneously operate in response to an address signal. Try state buffers enter an enable state in response to a testing mode signal. Accordingly, the outputs of the two logic circuits are output to a signal line through the try state buffers. When the two logic circuits are both nondefective, a supply current cannot be measured by a current measuring unit, but when one of the logic circuits is defective, an excessive supply current is measured by the current measuring unit, and hence, it can be determined that one of them is defective. Accordingly, a plurality of logic circuits can be simultaneously found defective or nondefective by the IDDQ testing, resulting in reducing time required for the testing.